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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,539	01/27/2004	Yoshikazu Saitoh	843.40341CX1	9621

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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-9889

EXAMINER	
NGUYEN, TAN	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,539	SAITOH ET AL.	
	Examiner	Art Unit	
	Tan T. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-24 and 27* is/are rejected.

7)☒ Claim(s) *25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/906,060.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

2. The Preliminary amendment submitted by Applicant on April 30, 2004 has been received and entered.

3. The Information Disclosure Statement submitted by Applicants on January 27, 2004 has been received and fully considered.

4. Claims 1-8 have been canceled.

New claims 9-27 have been added.

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 9-22 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 5, 6 and 1-4 of U.S. Patent No. 6,711,075. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 5, 6 and 8 of U.S. Patent No. 6,711,075 recites the same limitations such as the first terminal, the second terminal the memory matrix in claim 9 of the present application; the plurality of semiconductor chips, each of which

has a memory matrix, a plurality of address input terminals, a plurality of data input/output terminals, a plurality of control signal terminals, a plurality of test-only terminals in claim 13 of the present application; a memory circuit having a memory matrix, a test circuit in claim 16 of the present application.

The differences between claim 9 of the present application from claim 5 of U.S. Patent No. 6,711,075 are claim 9 recites a further terminal and the first terminal is coupled to receive a signal for judging electric connection/non-connection between a needle coupled to a test apparatus and the further terminal provided in each of the chip areas, while claim 5 of U.S. Patent No. 6,711,075 recites the first terminal inputting a signal for judging the electric connection/non-connection between a needle and a terminal provided in each of the semiconductor chips. This terminal would be understood as the claimed further terminal in claim 9 of the present application.

The difference between claim 13 of the present application from claim 6 of U.S. Patent No. 6,711,075 is claim 13 recites the test-only signal terminals for inputting signals for judging electric connection/non-connection while claim 6 of U.S. Patent No. 6,711,075 recites a plurality of test-only signal terminals are provided for judging electric connection.

The difference between claim 16 of the present application from claim 8 of U.S. Patent No. 6,711,075 is claim 16 of the present application recites a terminal, a test circuit for receiving a signal for judging the electric connection/non-connection between a needle and the terminal, and providing a response signal and based on the response signal judging electric connection/non-connection, while claim 8 of U.S. Patent No.

6,711,075 recites a test circuit for inputting a signal for judging electric connection/non-connection between a needle and a terminal. This terminal would be understood as the claimed terminal in claim 16. Furthermore, claim 8 recites the test circuit outputting a response signal for responding to the input signal (to the test circuit) and judging electric connection/non-connection between the needle and the terminal of the semiconductor chip.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the semiconductor wafer in claims 5, 6, 8 of U.S. Patent No. 6,711,075 by modifying the language in these claims from inputting to for receiving or to receive.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to modify the language from "a first terminal inputting" or "a test circuit inputting" to "a first terminal is coupled to receive" or "a test circuit for receiving", respectively, to clarify the language in the claims since a terminal, by itself, would receive a signal, but not generating or inputting a signal.

Regarding claim 17 of the present application, claim 1 of U.S. Patent No. 6,711,075 recites the test circuit is comprised of a test clock terminal, a first and second test control terminals, a test input/output terminal, a first power terminal and a second power terminal as similar to the limitations in claim 17 of the present application.

Regarding claims 10-11, 14-15 and 18 of the present application, the type of memory in the memory matrix is a matter of choice. A person of ordinary skill in the art

would have been motivated to select an appropriate memory type for the specific application.

Regarding claim 12 of the present application, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the semiconductor in claim 5 of U.S. Patent 6,711,075 by providing the semiconductor chip the test input/output external chip terminal as the terminal in the claim.
The rationale is as follows: A person of ordinary skill the art would have been motivated to use the test input/output external chip terminal to receive and to transmit test data.

Regarding claim 19 of the present application, claim 1 of U.S. Patent No. 6,711,075 recites the test circuit synchronizes the test clock signal with a combination of the test control signals, a shift register and a decoder similar to the limitations claimed in claim 19 of the present application.

Regarding claim 20 of the present application, claim 2 of U.S Patent No. 6,711,075 recites the test circuit having a counter and how the counter operates similar to the counter claimed in claim 20 of the present application.

Regarding claim 21 of the present application, claim 3 of U.S. Patent No. 6,711,075 recites the carry signal of the counter is used as write data of the memory circuit which is similar to the limitation in claim 21 of the present application.

Regarding claim 22 of the present application, claim 4 of U.S. Patent No. 6,711,075 recites how the carry signal of the counter and the read data of the memory circuit are operates by exclusive OR and the result is used to monitor bad rate during burn-in test similar to the limitation in claim 22 of the present application.

7. Claims 23-24 and 27 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. 6,711,075. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 14 of U.S. Patent No. 6,711,075 recites a manufacturing method of a semiconductor device wherein first and second semiconductor chips are cut out from different semiconductor wafers, and a contact check is performed in each of the first and second semiconductor chips.

Claim 14 of U.S. Patent No. 6,711,075 did not discuss the step of producing first and second wafers and assembling one of the first semiconductor chip and one of the second semiconductor chip to produce the semiconductor device.

It is inherent that a large amount of wafers are formed and tested to produce the semiconductor chips, and these chips are put together to form a desired semiconductor device.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the manufacturing method disclosed in claims 13-14 of U.S. Patent No. 6,711,075 to assemble a desired semiconductor device from a plurality of semiconductor chips which are cut out from separated wafers.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to assemble a desired semiconductor device from a plurality of semiconductor chips to save the manufacturing cost and time.

8. Claims 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

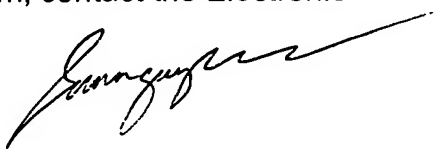
9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ban et al. and Hsuan et al. are cited to show fabrication methods in which a plurality of semiconductor modules are cut out and assembled after being tested.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms, can be reached at (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tan T. Nguyen
Primary Examiner
Art Unit 2818
July 27, 2004